PAPER

A Design of 0.7-V 400-MHz Digitally-Controlled Oscillator

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SUMMARY We present a low-voltage digitally-controlled oscillator (DCO) with the third-order ΔΣ modulator utilized in the medical implant communication service (MICS) frequency band. An optimized DCO core operating in the subthreshold region is designed, based on the g_m/I_D methodology. Thermometer coder with the dynamic element matching and ΔΣ modulator are implemented for the frequency tuning. High frequency resolution is achieved by using the ΔΣ modulator. The ΔΣ-modulator-based LC-DCO implemented in a 130-nm CMOS technology has achieved the phase noise of −115.3 dBc/Hz at 200 kHz offset frequency with the tuning range of 382 MHz to 412 MHz for the MICS band. It consumes 700 μW from a 0.7-V supply voltage and has a high frequency resolution of 18 kHz.

key words: *digitally-controlled oscillator, ΔΣ modulator, dynamic element matching, data-weighted averaging, clocked averaging, CMOS, MICS*

1. Introduction

The aggressive scaling of CMOS technology has allowed not only the reduction in the physical size of an integrated circuit but also the ability to include more components onto a single die. Radio frequency (RF) transceivers for medical implantable devices require miniaturized forms with a long battery life and low power consumption. Implantable medical devices are usually preferred to be fully integrated on a single chip to realize easier surgery and encapsulation for better biocompatibility. The medical implant communication service (MICS) band in the frequency range of 402 MHz to 405 MHz with 300 kHz channel bandwidth is widely used for medical RF transceivers because the MICS band signals have reasonable propagation characteristics in the human body and are well suited for achieving a good trade-off between the size and power [1]. Furthermore, the use of the MICS band does not pose a significant risk of an interference to other radio frequencies within or close to this band. Battery life time lasting longer without possibility of recharging is a challenge. The medical implantable devices must be optimized to consume as little energy as possible with achieving acceptable levels of performance.

Low power consumption and full integration are the most critical challenges for the design of implantable RF transceivers. After rapid growth over a decade in technology scaling, digital circuits have become preferable compared to analog circuits because of the aggressive cost, size, flexibility, and repeatability. The high level of integration demanded in wireless systems can be achieved with digital or digital-intensive approaches. RF oscillators, which traditionally use an analog approach for frequency tuning, now have digital interfaces to allow the peripheral circuitry to be implemented in a digital manner. A digitally-controlled oscillator (DCO), which was proposed for wireless applications in [2], generates a signal whose frequency can be controlled by digital words. The DCO allows efficient implementation of the direct frequency modulation in an all-digital phase-locked loop (ADPLL). In the design of the DCO, the low level of spurs and high resolution are challenges for implementations of the ADPLL. Low phase noise and precise frequency resolution for channel selection are desirable for the high-performance fully-integrated ADPLL architecture for wireless communications. There have been many efforts to improve the phase noise performance by improving the Q factor of the oscillator, and to increase the frequency resolution by using a large number of capacitors.

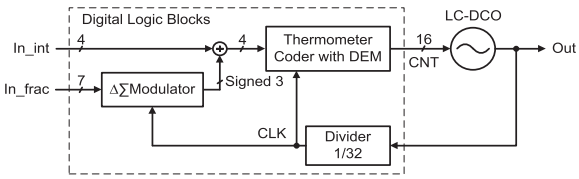

Fig. 1 Architecture of the DCO with the ΔΣ modulator.

In this work, the LC-DCO operating in the subthreshold region and ΔΣ modulator are employed for better performance. The CMOS devices operating in the subthreshold region have an advantage of higher transconductance to power dissipation ratio with a decent noise performance in comparison with the strong-inversion region. Therefore, the LC-DCO operating in the subthreshold region achieves low-power and low-phase-noise characteristics. Also, precise frequency resolution is achieved through the ΔΣ modulator. The structure of the employed ΔΣ modulator is a feedforward type which can reduce the noise spur.

This paper describes the ΔΣ-modulator-based LC-DCO design using a 130-nm CMOS process for the low-voltage operation. The architecture of a DCO operating in the MICS frequency band is shown in Fig. 1. It is composed of an LC-DCO core and the digital logic blocks for the

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frequency tuning. The oscillation frequency is controlled through the digital logic blocks with two types of digital word (In_int and In_frac). Thermometer coder with the dynamic element matching (DEM) is used for the conversion of an input digital bit. Also, for high frequency resolution, the ΔΣ modulator is employed and is clocked with the high frequency signal derived from the DCO output using a divide-by-32 circuit.

The focus is on the implementation details as well as measurement results. Section 2 presents the phase noise requirement and effect of the ΔΣ modulator using noise analysis. Section 3 describes the circuit design and implementation. The measurement results and comparison are presented in Sect. 4. Finally, conclusions are drawn in Sect. 5.

2. Phase Noise Analysis

2.1 Phase Noise Requirement for the MICS Band

The phase noise requirement for the MICS band oscillator is relatively relaxed. For MICS band receivers, because of the limited distance and upper bound of an equivalent isotropically radiated power, the dynamic range is determined by the path loss of around 30 dB at 2 m [3]. The MICS band has 10 channels and each channel occupies up to 300 kHz bandwidth [4]. If the frequency shift keying (FSK) modulation is used and the deviation of the two FSK tones is 50 kHz, then the closest adjacent channel interferer is at 200 kHz away from the carrier. Assuming a signal-to-noise ratio (SNR) of 15 dB is required by the FSK demodulation to obtain a bit error rate of 10^{-3}, the required phase noise at 200 kHz offset can be estimated using the following equation [5]:

$$L\{\Delta f\} = \frac{1}{\text{SNR (Path Loss) (Channel Bandwidth)}}, \quad (1)$$

where $L\{\Delta f\}$ is the phase noise at an offset frequency Δf. This gives the estimated phase noise as follows.

$$\begin{aligned} L\{200\text{ kHz}\} &= -15\text{ dB} - 30\text{ dB} - 10\log_{10}(300\text{ kHz}), \\ &= -100\text{ dBc/Hz}. \end{aligned} \quad (2)$$

The local oscillator signal should achieve under a phase noise of −100 dBc/Hz at an offset frequency of 200 kHz while suffering from an adjacent-channel interference.

2.2 Influence of ΔΣ Modulator on the Phase Noise

In this section, the extra phase noise introduced by quantization effects of ΔΣ modulator is analyzed. Generally, the noise transfer function (NTF) of an N-th order multi-stage noise shaping (MASH) ΔΣ modulator is given by [6]

$$NTF(z) = \left(1 - z^{-1}\right)^N. \quad (3)$$

The extra phase noise for the ΔΣ modulator, $L_{\Delta\Sigma_N}\{\Delta f\}$, is calculated as follows [7]:

$$L_{\Delta\Sigma_N}\{\Delta f\} = \frac{1}{12 f_{\Delta\Sigma}} \cdot \left(\frac{\Delta f_{res}}{\Delta f}\right)^2 \cdot |NTF(z)|^2, \quad (4)$$

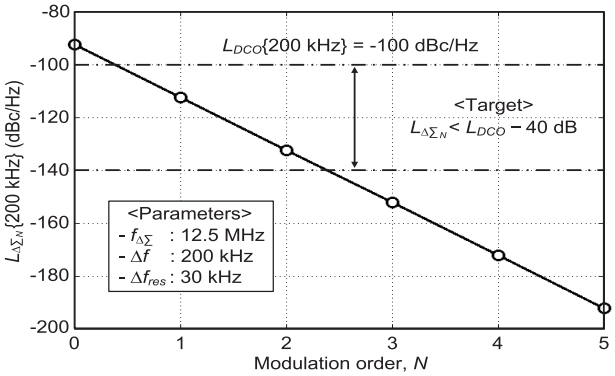


Fig. 2 Phase noise due to a modulation order.

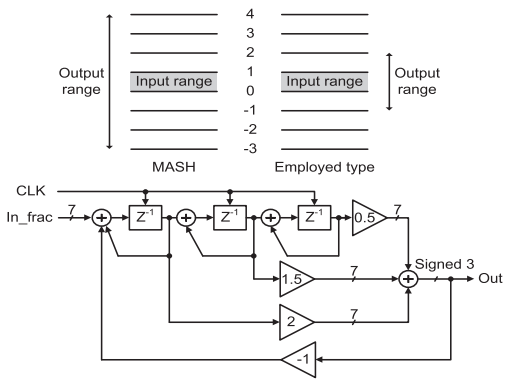


Fig. 3 Structure and output range of the third-order ΔΣ modulator.

where $f_{\Delta\Sigma}$ is the clock frequency of the ΔΣ modulator, and Δf_{res} is the frequency resolution associated with the effective capacitance switched by the ΔΣ modulator output. From this formula, it can be seen that both small frequency resolution and high clock frequency of the ΔΣ modulator are desirable for low-phase-noise contribution. In case of an N-th order ΔΣ modulator,

$$L_{\Delta\Sigma_N}\{\Delta f\} = \frac{1}{12 f_{\Delta\Sigma}} \cdot \left(\frac{\Delta f_{res}}{\Delta f}\right)^2 \cdot \left|2\sin\frac{\pi\Delta f}{f_{\Delta\Sigma}}\right|^{2N}. \quad (5)$$

Figure 2 shows the expected extra phase noise of the ΔΣ modulator as a function of modulation order N. The spurious tones can be reduced for the high-order ΔΣ modulator. However, the high-order ΔΣ modulator also increases the hardware complexity. To avoid the influence of the ΔΣ modulator on the phase noise performance, the target of extra phase noise is set below −40 dB than main oscillator phase noise. So, the third-order ΔΣ modulator is employed.

In this work, to avoid overflow and have a small output range, the feedforward structure as shown in Fig. 3 is used instead of the MASH structure. The shaded area in Fig. 3 represents the fractional input range. The number of output levels is only 4 while that of the MASH modulator is 8. Therefore, the feedforward structure is useful to prevent the drastic changes of the number of selected capacitors. The maximum quantization noise is also much less than the conventional MASH modulator. The NTF of the

employed modulator is given by [8]

$$NTF(z) = \frac{(1-z^{-1})^3}{1-z^{-1}+0.5z^{-2}-0.1z^{-3}}. \quad (6)$$

Substituting Eq. (6) into Eq. (4), the final extra phase noise for the third-order ΔΣ modulator is given by

$$L_{\Delta\Sigma_{3rd}}\{\Delta f\} = \frac{(\Delta f_{res}/\Delta f)^2}{12\, f_{\Delta\Sigma}} \cdot \frac{(2\sin(\pi\Delta f/f_{\Delta\Sigma}))^6}{1.06-2.5\,\rho+2.4\,\rho^2-0.8\,\rho^3}, \quad (7)$$

where ρ=cos($\pi\Delta f/f_{\Delta\Sigma}$). The calculated extra phase noise by the ΔΣ modulator is −150 dBc/Hz at condition of Δf=200 kHz, $f_{\Delta\Sigma}$=12.5 MHz, Δf_{res}=30 kHz, and N=3. The overall phase noise including the ΔΣ modulation is expressed as follows:

$$L_{\Delta\Sigma-DCO}\{\Delta f\} = L_{DCO}\{\Delta f\} + L_{\Delta\Sigma_N}\{\Delta f\}, \quad (8)$$

where $L_{DCO}\{\Delta f\}$ is the phase noise of the DCO core without the ΔΣ modulation at an offset frequency Δf. This gives $L_{\Delta\Sigma-DCO}$ {200 kHz}=−99.9 dBc/Hz. Clearly, the ΔΣ modulator introduces an extra phase noise through quantization noise. However, it hardly affects the overall phase noise because it is sufficiently as low as only 0.1 dB difference for MICS frequency band applications.

3. Circuit Design and Implementation

In this section, the circuit design methodology and parameters are discussed. Table 1 shows the design target specifications based on the MICS band requirements. Compared between the low-frequency oscillator and high-frequency oscillator with the frequency divider, the oscillator designs have a trade-off relation between the area occupation and power consumption, as shown in the literature [9]. In this design, the direct 400 MHz LC-DCO structure is considered for the low power consumption, as shown in Fig. 4. An NMOS cross-coupled pair is chosen for the oscillator core design operating at a 0.7-V supply voltage, because it has an advantage of the common-mode noise suppression and low-voltage operation. For the current biasing, top resistive biasing is applied to achieve lower phase noise at low-voltage operation. The switchable capacitor bank controlled by digital blocks is employed for the frequency tuning. In the output stage, CMOS buffers are employed to isolate the oscillator from output load variations and to provide the required output signal. An oscillator design procedure can be illustrated as follows.

Table 1 Design considerations

Technology	130-nm CMOS process
Supply voltage	0.7 V
Operating frequency	402 ~ 405 MHz (MICS band)
Tuning range	> 3 MHz
Frequency resolution	< 30 kHz
Phase noise	< −100 dBc/Hz @ 200 kHz offset
Power consumption	< 1 mW

1. LC tank
   - Determine the inductor with large Q factor value at center frequency.
   - Design the capacitor bank in accordance with the inductance to cover the frequency tuning range.
2. Oscillation core
   - Determine the bias current from the target power dissipation for a given supply voltage.
   - Calculate the target transconductance (g_m) specification from the parallel resistance of the LC tank.
   - Determine the transistor gate length from the unity-current-gain cut-off frequency f_T and current efficiency g_m/I_D (I_D: drain current).
   - Determine the transistor gate width to meet the required g_m from the g_m/I_D.

3.1 LC Tank and Digital Frequency Tuning

The DCO oscillation frequency is determined by the tank inductance and capacitance. Meanwhile, the tank loss, usually characterized by its Q factor, is the fundamental limitation on the achievable phase noise performance. So, maximizing the Q factor value of the tank inductor is an efficient way of reducing the phase noise through increasing oscillation amplitude. In this design, the dual-layer spiral inductor and switchable capacitor bank are used for an LC tank circuit. The dual-layer spiral inductor has a high Q factor value because of its lower series resistance [10]. The inductance and Q value of the spiral inductor are 8.18 nH and approximately 8 at 400 MHz, respectively. The oscillation frequency of the LC tank is calculated as follows:

$$f_0 = \frac{1}{2\pi\sqrt{L_{tot}C_{tot}}}, \quad (9)$$

where L_{tot}(=2L) and C_{tot} are total inductance and total capacitance, respectively. For the low-voltage operation, the frequency tuning of the LC-DCO using MOS varactors is an extremely challenging task due to its high nonlinear characteristics [2]. In this design, the switchable capacitor bank is utilized instead of the MOS varactor because it has a high Q factor, linear characteristics, and lower temperature coefficients than the varactor. Although low-cost

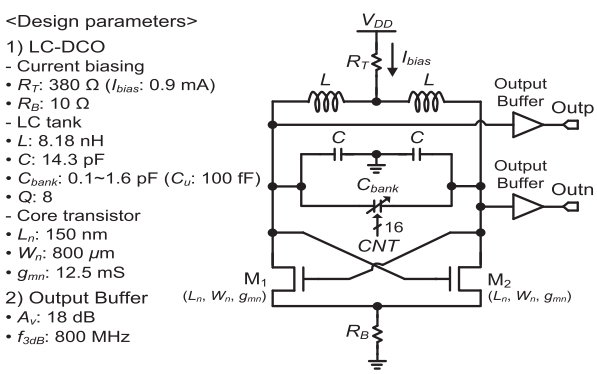


Fig. 4 Schematic of the LC-DCO.

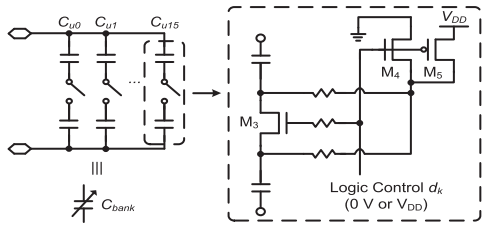


Fig. 5 Schematic of the switchable capacitor bank.

high-density metal-oxide-metal capacitors [11] can be fabricated, the stacked metal-insulator-metal (MIM) capacitors are used in this design considering predictability of a capacitor mismatch. The stacked MIM capacitor with a dual-layer can achieve high capacitance density. Figure 5 shows the schematic of the switchable capacitor bank. Each capacitor is switched by using an NMOS switch (M_3) which has a small parasitic capacitance because its on-state conductance can be enhanced even for a small gate width by controlling its source and drain voltages by M_4 and M_5 [12].

The frequency tuning with the switchable capacitor bank enables a fully digital implementation. As the main capacitors have a small capacitance due to the employed large inductor, the unit capacitors should have much smaller capacitance. The issue is that both small frequency steps and a wide frequency range must be realized with many bits. As classical implementations of capacitor arrays would require impractically tiny capacitors in the CMOS process, the $\Delta\Sigma$ modulator is utilized to achieve small effective capacitor step sizes. The total instantaneous capacitance can be expressed as below

$$C_{tot} = \frac{1}{2}\left[C + \left(\sum_{k=0}^{N_C-1} d_k\right) \cdot C_u\right], \tag{10}$$

where C is the main capacitance and C_u is the unit capacitance per control code. N_C represents the number of unit capacitors. The codes $\{d_k\}$ (CNT in Fig. 1) are generated in the thermometer coder with DEM in Fig. 1, and d_k indicates the deselection and selection of the k-th unit capacitor for d_k= 0 and 1, respectively. The main capacitance corresponding to the inductance is 14.3 pF, and the unit capacitance corresponding to the tuning range is 100 fF.

The frequency tuning specifications for the DCO are derived from the intended application with a periodic calibration, where the MICS reference tolerance is 100 ppm [3]. Accordingly, the target frequency resolution considering margin is set below 30 kHz. The oscillation frequency is decided by integer and fractional frequency tuning steps. The integer tuning step with 4-bit resolution covers a large frequency range with a calibration of the large frequency uncertainty due to process, voltage and temperature variations. The frequency resolution of the integer step Δf_I is 2 MHz. For precise channel selection, the fractional tuning step is utilized, which is realized by the $\Delta\Sigma$ modulator in this work, as shown in Fig. 1. The fractional tuning step with 7-bit resolution satisfies the target frequency resolution (< 30 kHz)

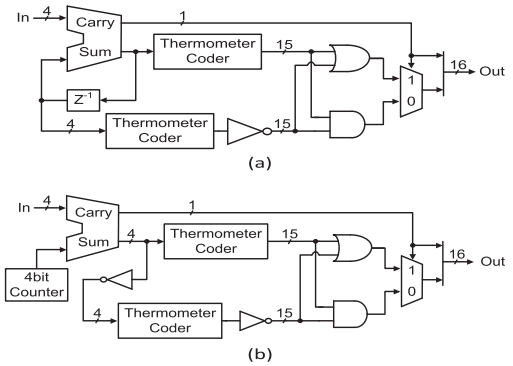


Fig. 6 Block diagram of (a) DWA and (b) CLA.

to cover narrower band range. The frequency resolution of the fractional step Δf_F is 18 kHz.

The effect of a capacitor mismatch in the switchable capacitor bank shown in Fig. 5 causes distortion in the oscillation signal. The DEM effectively eliminates component mismatches [13]. This technique rearranges the interconnections of the mismatched components to nearly equalize the time averages of the equivalent components at each of the component positions. The influence of the capacitor mismatch can be reduced by changing the capacitor selection during each time in DEM techniques [14]. Accordingly, the oscillation frequency is more stable due to reduction of the capacitor mismatch. There are many ways to realize the DEM. In this work, the data-weighted averaging (DWA) and clocked averaging (CLA) are considered for the DEM technique.

The designed DWA and CLA structures are shown in Figs. 6 (a) and (b). The DWA is the most widely used DEM technique due to its simplicity and low hardware overhead [15]. The DWA guarantees that each of the elements is used with an equal probability for each digital input code. To realize this, selecting elements sequentially begins with the next available unused element. On the other hand, the CLA is realized by sequentially selecting elements shifted by one element, and thereby the influence of previous selected capacitance remains. Compared with CLA, the instantaneous capacitance in DWA has a sudden change. So, the noise power from the mismatch is distributed at high frequency components. Moderate change of the instantaneous capacitance in CLA causes the noise power from the mismatch at low-frequency components. In this work, the DEM effect on the capacitor bank is compared between the DWA and CLA.

3.2 Oscillator Core

The CMOS devices operating in the subthreshold region provide high transconductance for a given bias condition. This property may be utilized to design low-power circuits. Since the transconductance g_m increases at the expense of lower unity-current-gain cut-off frequency f_T under constant drain current I_D, the subthreshold operation is desirable for

low-frequency applications. With a 130-nm CMOS technology, the device can be driven in the subthreshold region to achieve the highest transconductance for 400 MHz operation. To satisfy the oscillation condition in Fig. 4, the required device transconductance g_{mn} that satisfies unity loop gain at the oscillation frequency $f_0(=\omega_0/2\pi)$ is obtained from the following equations:

$$G_M \geq 1/R_p, \tag{11}$$

$$R_p \approx \omega_0 L_{tot} Q_L, \tag{12}$$

where R_p is the equivalent parallel resistance of an LC tank, Q_L is the Q factor of an inductor, and $G_M(=g_{mn}/2)$ is the transconductance of the NMOS differential-pair M_1 and M_2. In practice, a loop gain of 1.5 to 3 is often used to ensure the start-up for the oscillation. The required transconductance overcoming equivalent parallel tank resistance of an LC tank ($R_p \approx 330\ \Omega$) is set to 6 mS with a safety factor of 2 for the stable oscillation including the start-up condition, and actual transconductance for NMOS devices M_1 and M_2 (g_{mn}) is set to 12 mS. The NMOS devices are designed in the subthreshold region to satisfy the required transconductance specification.

The NMOS saturation drain current in the subthreshold region is proportional to the exponential of the gate-source voltage V_{GS}, which is expressed as

$$I_D \approx I_{D0} \frac{W_n}{L_n} e^{\frac{V_{GS}-V_{TH}}{nU_T}}, \tag{13}$$

where W_n/L_n is the device aspect ratio, I_{D0} is the technology current, V_{TH} is the threshold voltage. n is the subthreshold slope factor, $U_T=k_BT/q$ is the thermal voltage, k_B is the Boltzmann's constant, T is the absolute temperature, and q is the electronic charge (U_T=25.9 mV at room temperature). The transconductance in this region is expressed as

$$g_m = \frac{I_D}{nU_T}. \tag{14}$$

In this region, the drain current is mainly diffusion current and the device works like a bipolar transistor.

The g_m/I_D methodology has been an attractive technique as a transistor sizing tool for low-power designs since the current efficiency g_m/I_D indicates a measure of efficiency to generate g_m from a given I_D. The g_m/I_D can specify all device operation regions including the strong, moderate, and weak inversion regions [16]. The fundamental design parameters, the unity-current-gain cut-off frequency f_T and current efficiency g_m/I_D, are calculated as a function of the current density I_D/W_n for various channel lengths. The f_T corresponds to $g_m/2\pi C_{gg}$, where C_{gg} is the total capacitance at gate node, and depends on the device size.

Figure 7 demonstrates the f_T for various channel lengths against the I_D/W_n for a 130-nm CMOS process. It is confirmed that the f_T decreases with reduced I_D/W_n and increased channel length due to the gate node capacitance ($C_{gg} \propto L_n W_n C_{ox}$, C_{ox} is the gate-oxide capacitance per unit dimension). In the subthreshold region, it has a low f_T, which is associated with low-frequency applications.

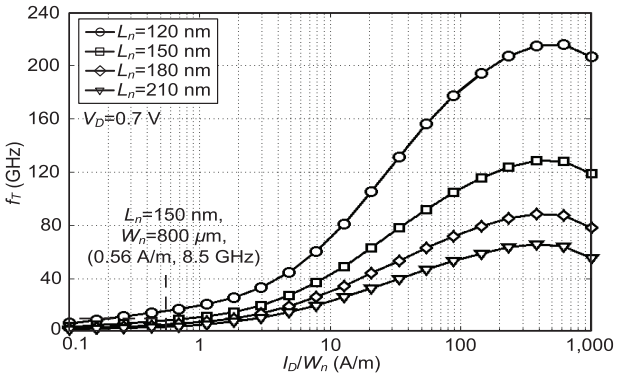


Fig. 7 Unity-current-gain cut-off frequency f_T versus I_D/W_n ratio for different channel lengths.

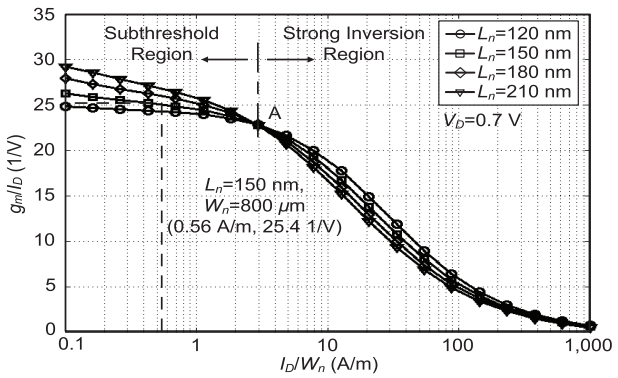


Fig. 8 Current efficiency g_m/I_D versus I_D/W_n ratio for different channel lengths.

Figure 8 demonstrates the simulated g_m/I_D against the I_D/W_n ratio with different channel lengths for the 130-nm CMOS process. It is observed that the g_m/I_D gradually reduces with the I_D/W_n ratio. From the square-law device model in the strong inversion, the g_m/I_D can be derived as the $2/V_{OV}$ where the overdrive voltage $V_{OV}=V_{GS}-V_{TH}$. Reduced I_D/W_n enhances the g_m/I_D through decreased V_{OV}. Also, the short-channel devices in the strong inversion region have higher transconductance due to increase of the lateral electric field [17]. At the transition point A, the V_{OV} value decreases to under zero by reducing I_D/W_n ($V_{OV}<0$). In the subthreshold region, the g_m/I_D degrades with the reduction of the gate length L_n, which originates from the degradation of the sensitivity of the surface potential to gate voltage [18] and in other word, an increase in n in Eq. (14).

Considering the required transconductance, the channel length L_n as 150 nm and width W_n as 800 μm are used for the NMOS pair transistors. In this design point, the g_{mn} and f_T are approximately 12 mS and 8.5 GHz, respectively. It has enough f_T to operate in the MICS frequency band.

For the current biasing, the resistive biasing with the resistor R_T is applied. This technique is more suitable than active current mirror biasing technique because of the inherent advantage of the low-noise and large output voltage

swing. Also, the noise performance is improved by eliminating the noise from the active current mirror source [19]. For the low power consumption, the target of current consumption is set below 1 mA. The top bias feeding resistance is approximately 380 Ω and its thermal noise has a small influence on the phase noise. In addition, to obtain the common-mode rejection, the bottom resistor with a small value (R_B=10 Ω) is also utilized.

4. Experimental Results and Comparison

Figure 9 shows the die photograph of the ΔΣ-modulator-based LC-DCO fabricated in a 130-nm CMOS process with a 0.7-V supply voltage which is the minimum voltage for the stable operation of the employed digital standard-cell circuits. The total chip area including pads is 1.96 mm^2, and the active chip area is about 0.41 mm^2. The total power consumption of the fabricated ΔΣ-modulator-based LC-DCO is 700 μW where the DCO core and digital blocks consume 630 μW and 70 μW, respectively.

Figure 10 shows the measured phase noise performance of the ΔΣ-modulator-based LC-DCO by DEM techniques. The digital logic blocks for the frequency tuning introduce the spurious based on the quantization noise. So, the total phase noise of the DCO includes both the DCO core noise and spurious from the digital logic blocks. In the digital logic blocks, the ΔΣ modulator and DEM generate the spurious tone at an offset of similar and lower than the CLK frequency, respectively. Therefore, the DEM spur affects more the phase noise performance in the MICS band. Compared with DEM methods, the CLA spur is generated at lower frequency offset than the DWA spur (DWA spur: −75 dBc/Hz @ 6 MHz offset, CLA spur: −73 dBc/Hz @ 800 kHz offset). This trend corresponds to the simulated phase noise of the CLA and DWA in Figs. 8 (a) and (b) of [14]†. Even if the spurious tone is introduced, it does not affect the phase noise performance because the spurious tone is generated at a large offset frequency out of the MICS channel bandwidth (300 kHz). Also, the generated spurious tone satisfies the permitted spurious emission level, which is 30 dB lower than transmitter power [3]. The measured phase noise results are −96.9, −115.3, and −118.6 dBc/Hz at 100 kHz, 200 kHz, and 1 MHz offsets, respectively. It satisfies the MICS band requirement (L{200 kHz}<−100 dBc/Hz).

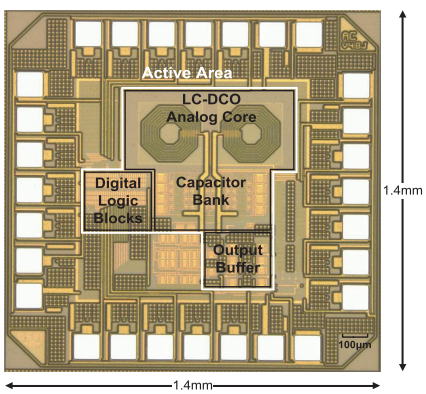
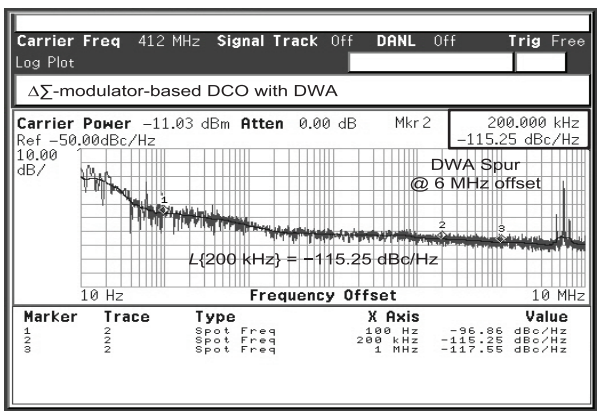


Fig. 9 Die photograph.

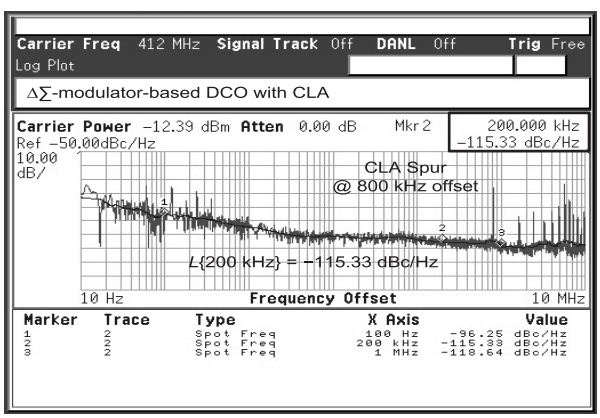
The oscillator is tuned by two types of digital control word as integer and fractional codes. Figure 11 shows the measured DCO frequency tuning range. Implemented LC-DCO has an integer frequency tuning range from 382 MHz to 412 MHz. It has a wide tuning range and covers the MICS frequency band. The frequency resolution of the integer tuning by 4-bit is roughly 2 MHz. The fractional frequency tuning range is achieved by using the ΔΣ modulator. To obtain the precise fractional tuning range, the measured data for the same codes are averaged. The fractional frequency resolution is roughly 18 kHz, and it satisfies the target of the MICS band frequency tolerance.

To evaluate this work, the well-known figure-of-merits (FoMs) are employed as shown below [20]

$$\mathrm{FoM} = L\{\Delta f\} - 20\log_{10}\left(\frac{f_0}{\Delta f}\right) + 10\log_{10}\left(\frac{P_{diss}}{1\ \mathrm{mW}}\right), \tag{15}$$



(a)



(b)

Fig. 10 Measured phase noise of the ΔΣ-modulator-based DCO with (a) DWA and (b) CLA.

†We found Figs. 8 (a) and (b) were replaced each other in the previous paper [14]. This correction does not affect the content of [14].

Table 2 Performance summary and comparison

	This work	[21]	[22]	[23]	[24]
Technology	130-nm	180-nm	65-nm	130-nm	180-nm
Supply voltage	0.7 V	0.7 V	1.0 V	1.2 V	1.5 V
Type	11-b LC-DCO	7-b LC-DCO	LC-VCO	LC-VCO	LC-VCO
Center frequency	397 MHz	403 MHz	403 MHz	403 MHz	395 MHz
FTR	7.6 %	2.5 %	1.2 %	1.2 %	22 %
Phase noise	−115 dBc/Hz @ 200 kHz offset	−118 dBc/Hz @ 1 MHz offset	−102 dBc/Hz @ 200 kHz offset	−96 dBc/Hz @ 100 kHz offset	−98 dBc/Hz @ 160 kHz offset
Power	700 μW	400 μW	430 μW	720 μW	1.87 mW
FoM	−182.8 dBc/Hz	−174.1 dBc/Hz	−171.8 dBc/Hz	−169.5 dBc/Hz	−163.3 dBc/Hz
FoM_T	−180.4 dBc/Hz	−161.9 dBc/Hz	−153.7 dBc/Hz	−151.4 dBc/Hz	−170.2 dBc/Hz

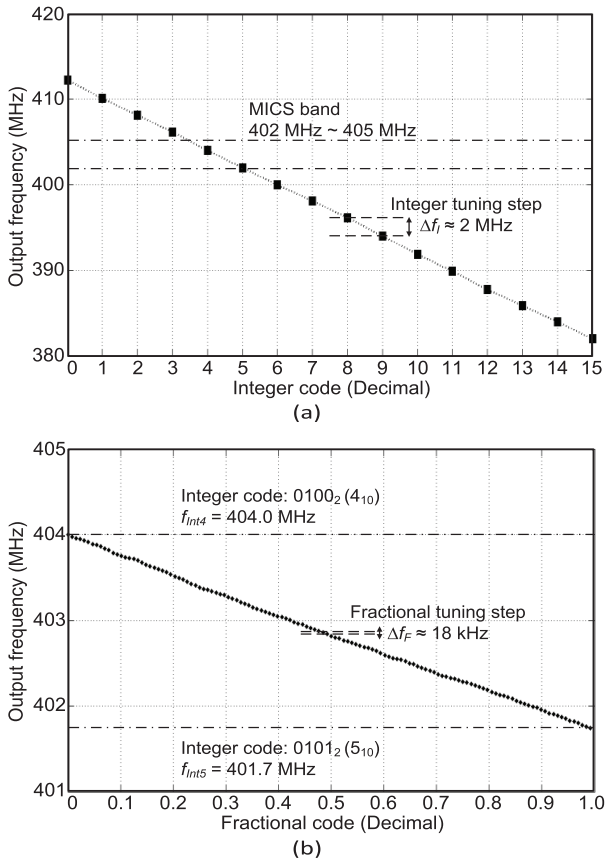


Fig. 11 Measured DCO frequency range of (a) integer tuning and (b) fractional tuning.

$$\text{FoM}_\text{T} = \text{FoM} - 20\log_{10}\left(\frac{\text{FTR}}{10\ \%}\right), \tag{16}$$

where f_0 is the oscillation frequency, P_{diss} is the power dissipation, and FTR is the frequency tuning range in percent. The FoMs are normalized at an offset frequency. Table 2 shows performance summary and the comparison of this work with respect to the oscillators in the MICS frequency band reported in the literature. Compared with the related works, this work has better phase noise performance and wide tuning range with high frequency resolution. Low phase noise is realized by the subthreshold operation and resistive biasing technique. The wide frequency tuning range is achieved through the switchable capacitor bank controlled by the digital logic blocks. This technique also improved the linearity and resolution. The use of the $\Delta\Sigma$ modulator achieved a precise frequency resolution with a small number of capacitors.

5. Conclusion

In this work, a low-voltage design of the $\Delta\Sigma$-modulator-based LC-DCO for the MICS band application is presented. The design of the DCO core is optimized by the g_m/I_D methodology for the low-voltage operation. The resistive biasing technique is employed for advantage of the low-noise and large output voltage swing. The digital frequency tuning with the precise frequency resolution is implemented in the digital logic blocks, such as thermometer coder with the DEM (DWA and CLA) and $\Delta\Sigma$ modulator. The DEM technique effectively reduces the influence of the capacitor mismatch. From the measurement results, it is confirmed that the fabricated DCO has a low phase noise and precise frequency resolution.

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